We claim:

1. A method for forming a ferroelectric capacitor comprising:

providing a dielectric layer over a semiconductor;

forming a barrier layer over said dielectric layer;

forming a first metal layer over said barrier layer;

forming a ferroelectric layer over said first metal layer;

forming a second metal layer over said ferroelectric layer;

forming a hard-mask layer over said second metal layer; and

etching said second metal layer, said ferroelectric layer, and said first metal layer using a plasma process performed at temperatures between 200°C and 500°C.

2. The method of claim 1 wherein said plasma process comprises a three step process, comprising:

a first metal layer etch comprising the gases Cl_2, O_2, N_2, and CO;

a PZT etch comprising the gases BCl_3 and Cl_2; and

a second metal layer etch comprising the gases Cl_2, O_2, N_2, and CO.

3. The method of claim 1 wherein said plasma process comprises a PZT etch process comprising the gases BCl_3 and Cl_2 in a range of ratios from 1:4 to 10:1 respectively.

4. The method of claim 2 wherein said first metal layer comprises iridium, said ferroelectric layer comprises PZT, and said second metal layer comprises iridium.

5. The method of claim 4 wherein said second metal layer comprises iridium.

6. A method for forming a ferroelectric memory cell comprising:

providing a dielectric layer over a semiconductor;

forming a barrier layer over said dielectric layer;

forming a first metal layer over said barrier layer;

forming a ferroelectric layer over said first metal layer;

forming a second metal layer over said ferroelectric layer;

forming a hard-mask layer over said second metal layer;

etching said first metal layer with a plasma process comprising the gases Cl_2, O_2, N_2, and CO; and

etching said ferroelectric layer with a plasma process comprising the gases BCl_3 and Cl_2.

7. The method of claim 6 wherein all etch process are performed at temperatures between 200°C and 500°C.

8. The method of claim 7 wherein said ferroelectric layer etch process further comprises the gases BCl_3 and Cl_2 in a range of ratios from 1:4 to 10:1 respectively.

9. The method of claim 8 wherein said first metal layer comprises iridium and said ferroelectric layer comprises PZT.

10. A method for forming a ferroelectric memory capacitor comprising:

providing a dielectric layer over a semiconductor wherein said dielectric layer has an upper surface forming a plane;

forming a barrier layer over said dielectric layer;

forming a first metal layer over said barrier layer;

forming a ferroelectric layer over said first metal layer;

forming a second metal layer over said ferroelectric layer;

forming a hard-mask layer over said second metal layer; and

etching said second metal layer, said ferroelectric layer, and said first metal layer using a plasma process to form sidewalls wherein the angle formed by said sidewalls and said plane is between 78° and 88°.

11. The method of claim 10 wherein said plasma process comprises a three step process, comprising:

a first metal layer etch comprising the gases Cl_2, O_2, N_2, and CO;

a PZT etch comprising the gases BCl_3 and Cl_2; and

a second metal layer etch comprising the gases Cl_2, O_2, N_2, and CO.

12. The method of claim 10 wherein said plasma process comprises a PZT etch process comprising the gases BCl_3 and Cl_2 in a range of ratios from 1:4 to 10:1 respectively.

13. The method of claim 11 wherein said first metal layer comprises iridium, said ferroelectric layer comprises PZT, and said second metal layer comprises iridium.

14. A ferroelectric memory cell, comprising:

a dielectric layer comprising an upper surface that forms a plane;

a metal contact formed in said dielectric layer;

a ferroelectric capacitor formed over said metal contact comprising:

a barrier layer;

a first metal layer;

a ferroelectric layer; and

a second metal layer wherein said ferroelectric capacitor has sidewalls such that the angle formed between said sidewalls and said plane is between 78° and 88°.

15. The ferroelectric capacitor of claim 14 wherein said sidewalls are formed by etching said barrier layer, first metal layer, said ferroelectric layer and said second metal

layer with plasma processes at temperatures between 200°C and 500°C.

16. The ferroelectric capacitor of claim 15 wherein said ferroelectric layer comprises PZT.

17. The ferroelectric capacitor of claim 16 wherein said PZT layer is etch using BCl_3 and Cl_2 in the ratios from 1:4 to 6:1 respectively.